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(Modified)

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

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APPLICATION NO.  
10/669,307

INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

APPLICANT Chia-Liang LIN

(Use several sheets if necessary)

(37 CFR 1.98(b))

FILING DATE  
September 23, 2003

GROUP ~~2631~~  
2819

U.S. PATENT DOCUMENTS

EXAM INIT	PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
JBJD	5,404,142	04/1995	Adams et al	341	144	—
JBJD	5,684,482	11/1997	Galton	341	144	—
JBJD	6,304,608	10/2001	Chen et al	341	143	—

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

EXAM INIT	DOCUMENT NUMBER	PUBL. DATE	COUNTRY OR PAT. OFFICE	CLASS	SUB CLASS	TRANS.	
						Y	N

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)

JBJD	WELZ, Jared; GALTON, Ian; and FOGLEMAN, Eric; "Simplified Logic for First-Order and Second-Order Mismatch-Shaping Digital-to-Analog Converters;" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS--II ANALOG AND DIGITAL SIGNAL PROCESSING; Vol. 48; No. 11; November 2001; Pgs. 1014-1027

EXAMINER

*Glan Bruner Glanland*

DATE CONSIDERED

5/28/04

EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.